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Multi-Source Solution for Intel® 28Fxx0B3 Advanced Boot Block and AMD 29LV160/800/400

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NOTE: This document formerly known as *Multi-Source Solution for Intel 28F160 Advanced Boot Block and AMD 29LV160.*

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
10/28/97	-001	Original Version
12/02/97	-002	Updated 4-Mbit package information Section 3.1.
12/01/98	-003	Major wording revision
		Added a description of 12 V Production Programming and In-System Hardware Block Locking
		Added a description of memory blocking differences
		Name of document changed from *Multi-Source Solution for Intel 28F160 Advanced Boot Block and AMD 29LV160* technical paper

1.0 INTRODUCTION

This application note outlines how to design a single socket to support the Intel® 3 Volt Advanced Boot Block (B3) and the AMD AM29LVxxx (LV) flash memory device. While the focus is on the 16-Mbit density, similar changes will be required for lower density devices. Note that a x8 cross reference design is not discussed in this paper because the x8 B3 devices are manufactured in 40-lead TSOP whereas x8 LV devices are provided in a 48-lead TSOP package.

Section 2 defines the advantages in designing with the B3 while Section 3 presents a single socket, multi-source solution.

2.0 3 VOLT ADVANCED BOOT BLOCK OVERVIEW

The B3 product is architected for low voltage (2.7 V – 3.6 V) applications requiring code execution and data storage within the same flash devices. The B3 consists of eight 8-KB blocks (at either the top or bottom location of the device) followed by several 64-KB blocks, depending on the density; 4-/8-/16-/32-Mbit. See the *3 Volt Advanced Boot Block* datasheet for details.

In addition the B3 offers the following design advantages when designing a multi-source solution:

- Pinout compatibility for easy density upgrade path
- 12 Volt Production Programming for fast programming during manufacturing
- Program suspend to read functionality for real time applications
- In-system hardware block locking
- A vast array of Intel Memory Managers and design tools to reduce time to market.

The following sections describe these features and advantages in more detail. Table 1 compares features offered by the B3 and the LV.

2.1 Pinout Compatibility

The B3 products provide density upgrades with pinout compatibility for the 4-, 8-, 16-, and 32-Mbit densities:

- The 48-ball µBGA* CSP package, ideal for space constrained designs, is available in 8-, 16-, and 32-Mbit densities for both x8 and x16 functionality
- The 48-lead TSOP is available in 4-, 8-, 16-, and 32-Mbit densities for x16 functionality
- The 40-lead TSOP is available in 4-, 8-, and 16-Mbit densities for x8 functionality

Pinout and package compatibility are extremely important for applications that may change their code or data requirements. Designing for compatibility reduces the impact of re-spinning the board and lengthens the application's life time. To accommodate changing requirements the design should be architected for the highest density flash device available and use the density that is required for the present design.

2.2 12 Volt Production Programming

The B3 products support production programming at 12 V to significantly reduce programming time in a manufacturing line. This may be combined with 2.7 V – 3.6 V in-system programming. Please refer to *the 3 Volt Advanced Boot Block Flash Memory* datasheet (order 290580) for details.

2.3 In-System Hardware Block Locking

The B3 offers in-system hardware block locking for the lower (upper) two 8-Kbyte parameter blocks for bottom (top) boot devices. The block locking may be done in-system by applying GND to WP# to lock the blocks or V_{IH} (min) to WP# to unlock the blocks. LV devices require an algorithm that uses 12 V to change the locking.

Additionally, when Vpp = GND, the entire device is write protected. LV devices do not separate the program/erase supply from the core power supply.

2.4 Program Suspend to Read Functionality

The B3 offers enhanced suspend capabilities. While both the B3 and the LV offer erase suspend to program or read, only the B3 offers program suspend to read for real time applications that require critical data within the maximum program time which may be as large as 100 µs.

2.5 Intel® Memory Managers and Design Tools

Intel offers several flash memory managers to reduce design time and offer quicker time to market solutions. For example, Flash Data Integrator used for code plus data real-time solutions.

Intel also offers a range of flash memory tools enable shorter development schedules with lower development costs. Tools are offered for every stage of system development.

For more information on software, please refer to the Intel® Flash website at http://developer.intel.com/ design/flash. Table 3 outlines software and tools supported by Intel and AMD.

Table 1. Feature Comparison Between B3 and LV

Feature	B3	LV
Pinout Compatibility	4-, 8-, 16-, 32-Mbit for 48-lead TSOP (x16)	2-, 4-, 8-, 16-Mbit for 48-Lead TSOP
	4-, 8-, 16-Mbit for 40-lead TSOP (x8)	2-, 4-, 8-, 16-Mbit for 44-Lead PSOP
	8-, 16-, 32-Mbit for 48-ball uBGA (x16 and x8)	
12 Volt Production Programming	Yes, 8 µs word write	No, 11 µs word write
Lower voltage I/Os	Yes, 1.65 V – 2.5 V	No, 2.7 V- 3.6 V
In-system hardware block locking	2.7 V – 3.6 V in system	Requires 12 V in system
Program suspend to read	Yes	No
Erase suspend to read	Yes	Yes
Erase suspend to program	Yes	Yes

Table 2. Offered/Supported Tools by Intel and AMD

Tools Available	Intel	AMD
Flash Media Managers and Software Drivers	Yes	No
Behavioral Models (VHDL and Verilog)	Yes	No
IBIS Models	Yes	No
TimingDesigner* Models	Yes	No
PCB Layout Files	Yes	No
Schematic Symbols	Yes	No

NOTE:

For information on these and other tools, organized by specific flash memory product, visit Intel's Website at http://www.intel.com.

3.0   DEVELOPING MULTI-SOURCED DESIGNS

This section describes the changes required to design a multi-source socket solution for the x16 16-Mbit B3 and LV. Similar methodologies may be applied for other densities.

Attention is required for the following differences:

- AC specifications
- Pinouts
- Blocking
- Command sets
- Command completion

3.1   AC Specification Differences

AC timing specification differences are outlined in Table 3. Note that address setup/hold times are different for the B3 vs. the LV because addresses are latched on different WE# edges (see Section 3.1.1 for details).

3.1.1   ADDRESS/DATA SETUP/HOLD TIMES

Address/data setup/hold times are dependent on when the information is latched internally. While the B3 and the LV devices both latch data on the rising edge of WE#, the B3 latches addresses on the rising edge of WE# whereas the LV latches addresses on the falling edge of WE# (see Figure 1).

Adequate address/data setup and hold timings must account for valid address/data being available at the proper edges when designing for both the LV and B3. One approach is to design the setup and hold timings such that the addresses and data are latched and held through both the rising and falling edges of WE#.

Table 3. AC Specification Differences Related to Address/Data Latching

Spec	Intel		AMD		Notes
Address Setup	t_{AVWH}	70 ns	t_{AVWL}	0 ns	This timing is from address valid to WE# high (for Intel) and to WE# low (for AMD).
Address Hold	t_{WHAX}	0 ns	t_{WLAX}	50 ns	45 ns for AMD –90 ns speed device
Data Setup	t_{DVWH}	50 ns	t_{DVWH}	50 ns	45 ns for AMD –90 ns speed device
Write Pulse Width	t_{WLWH}	70 ns	t_{WLWH}	50 ns	

Table 4. Other AC Specification Differences

Spec	Intel		AMD		Notes
OE# Delay	t_{GLQV}	30 ns	t_{GLQV}	50 ns	AMD –90 ns has t_{GLQV} = 30 ns
CE# Data Float	t_{EHQZ}	25 ns	t_{EHQZ}	30 ns	
OE# Data Float	t_{GHQZ}	25 ns	t_{GHQZ}	30 ns	
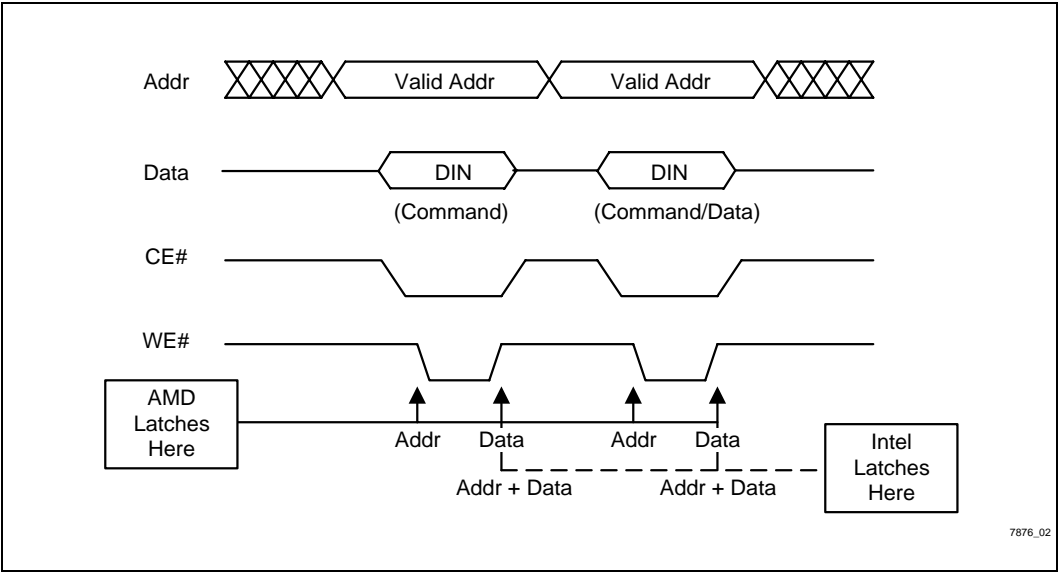
Figure 1. Differences in Address and Data Latching

3.2 Pinout Differences

The pinout differences (48-lead TSOP) between the B3 and the LV are shown in Figure 2. Pins that are No Connects (NCs) on one device will function properly when replaced with a device that assigns functionality to that pin. This is because NCs are not bonded to the die and therefore have no physical connection to the die. There are no compatibility issues as reflected in Table 6.

Two pins that require special attention are pins 15 and 47.

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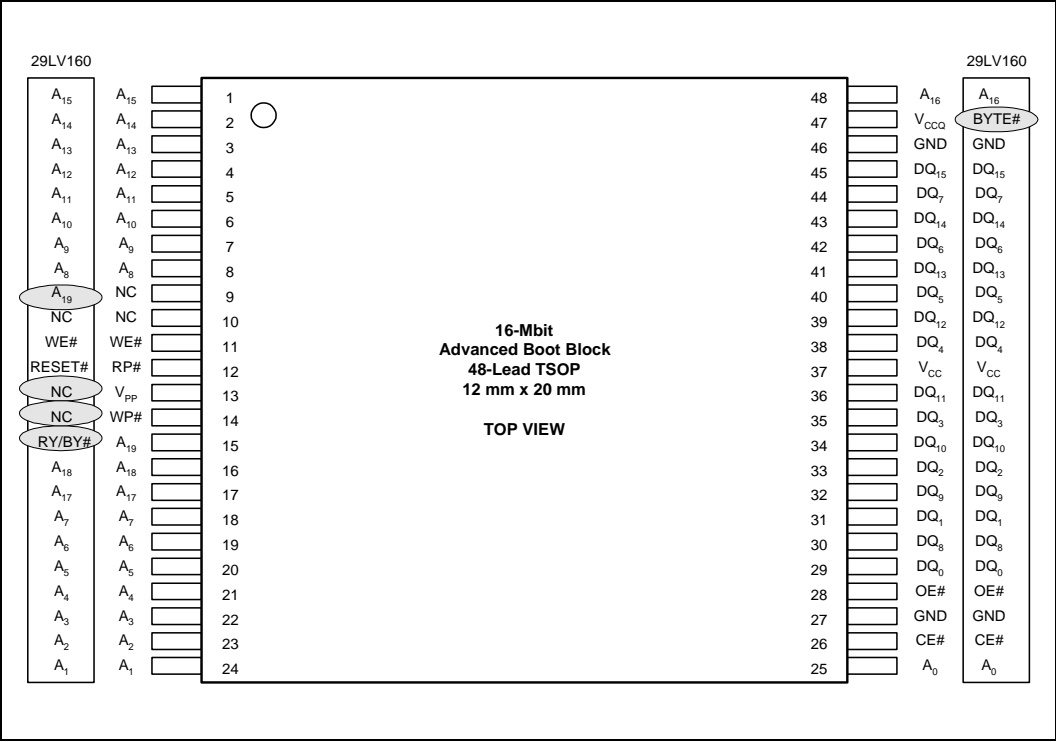
Figure 2. Comparison of 28F160B3 Advanced Boot Block 48-Lead TSOP Pinout Versus AMD 29LV160

Table 5. Comparison of Intel and AMD 48-Lead TSOP Pinout

Pin #	Intel	AMD	Issue (?)
9	NC	A_{19} (Address 19)	No
13	V_{PP}	NC	No
14	WP#	NC	No
15	**A_{19} (Address 19)**	**RY/BY#**	**Yes**
47	**V_{CCQ} (I/O voltage)**	**BYTE#**	**Must be between 2.7 V – 3.6 V for multi-source solutions**

Pin 15 is A_{19} on the B3, an input, and RY/BY# on the LV, an open drain output. This may cause bus contention if not properly handled. Figure 3 provides a design method to alleviate this concern using a simple 10 KΩ resistor.
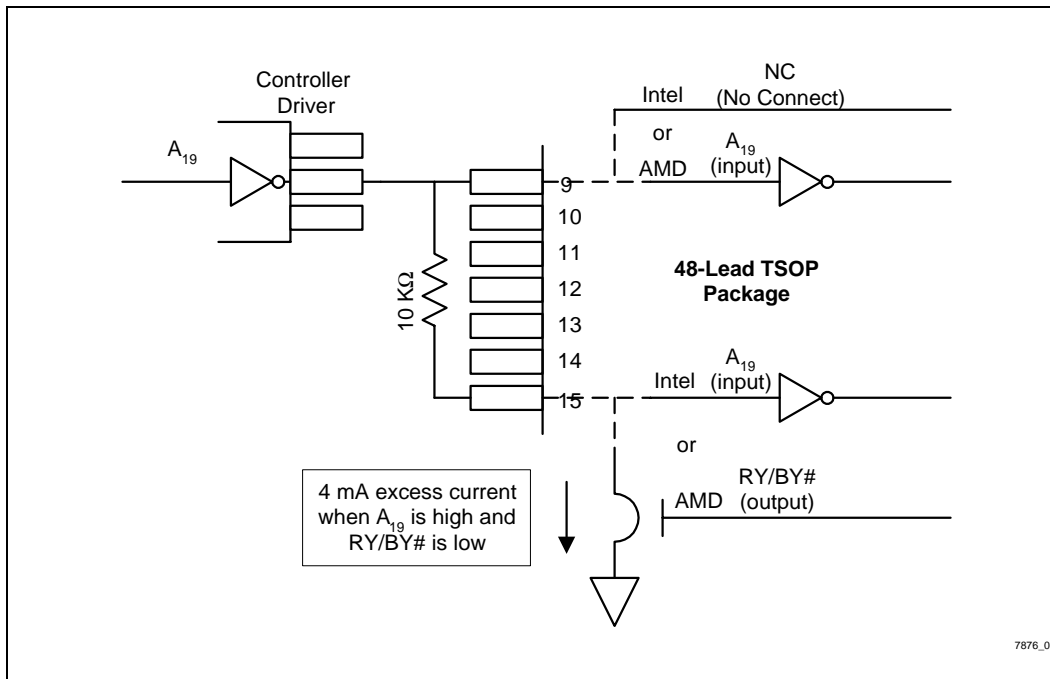
Figure 3. A Resistor Solution for Address A$_{19}$ (Intel) and RY/BY# (AMD)

Pin 47 is I/O supply pin on the B3, V$_{CCQ}$, and BYTE# pin on the LV. For a x16 multi-source design both must be between 2.7 V – 3.6 V. Lower voltage 1.65 V – 2.5 V I/O capability is not allowed in a multi-source solution because LV devices do not support this feature.

3.3   Blocking

B3 devices are architected with eight 4-Kword parameter blocks; the remainder of the array is divided into 32-Kword blocks. LV devices are architected with an 8-Kword, two 4-Kword, and a 16-Kword parameter blocks with the remainder of the array divided into 32-Kword blocks (see Table). Note that the LV blocking is a subset of the B3 blocking. Although the blocking architectures are similar, software must account for these parameter block differences. For example, when erasing the one 16-Kword block of the LV device, four 4-Kword blocks must be erased on the B3 to account for the same address range.

8-Mbit, 16-Mbit, and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	B3	Size (KW)	LV	Size (KW)	B3	Size (KW)	LV
4	FF000-FFFFF	8	FE000-FFFFF	32	F8000-FFFFF	32	F8000-FFFFF
4	FE000-FEFFF			32	F0000-F7FFF	32	F0000-F7FFF
4	FD000-FDFFF	4	FD000-FDFFF	32	E8000-EFFFF	32	E8000-EFFFF
4	FC000-FCFFF	4	FC000-FCFFF	32	E0000-E7FFF	32	E0000-E7FFF
4	FB000-FBFFF	16	F8000-FBFFF	32	D8000-DFFFF	32	D8000-DFFFF
4	FA000-FAFFF			32	D0000-D7FFF	32	D0000-D7FFF
4	F9000-F9FFF			32	C8000-CFFFF	32	C8000-CFFFF
4	F8000-F8FFF			32	C0000-C7FFF	32	C0000-C7FFF
32	F0000-F7FFF	32	F0000-F7FFF	32	B8000-BFFFF	32	B8000-BFFFF
32	E8000-EFFFF	32	E8000-EFFFF	32	B0000-B7FFF	32	B0000-B7FFF
32	E0000-E7FFF	32	E0000-E7FFF	32	A8000-AFFFF	32	A8000-AFFFF
32	D8000-DFFFF	32	D8000-DFFFF	32	A0000-A7FFF	32	A0000-A7FFF
32	D0000-D7FFF	32	D0000-D7FFF	32	98000-9FFFF	32	98000-9FFFF
32	C8000-CFFFF	32	C8000-CFFFF	32	90000-97FFF	32	90000-97FFF
32	C0000-C7FFF	32	C0000-C7FFF	32	88000-8FFFF	32	88000-8FFFF
32	B8000-BFFFF	32	B8000-BFFFF	32	80000-87FFF	32	80000-87FFF
32	B0000-B7FFF	32	B0000-B7FFF	32	78000-7FFFF	32	78000-7FFFF
32	A8000-AFFFF	32	A8000-AFFFF	32	70000-77FFF	32	70000-77FFF
32	A0000-A7FFF	32	A0000-A7FFF	32	68000-6FFFF	32	68000-6FFFF
32	98000-9FFFF	32	98000-9FFFF	32	60000-67FFF	32	60000-67FFF
32	90000-97FFF	32	90000-97FFF	32	58000-5FFFF	32	58000-5FFFF
32	88000-8FFFF	32	88000-8FFFF	32	50000-57FFF	32	50000-57FFF
32	80000-87FFF	32	80000-87FFF	32	48000-4FFFF	32	48000-4FFFF
32	78000-7FFFF	32	78000-7FFFF	32	40000-47FFF	32	40000-47FFF
32	70000-77FFF	32	70000-77FFF	32	38000-3FFFF	32	38000-3FFFF
32	68000-6FFFF	32	68000-6FFFF	32	30000-37FFF	32	30000-37FFF
32	60000-67FFF	32	60000-67FFF	32	28000-2FFFF	32	28000-2FFFF
32	58000-5FFFF	32	58000-5FFFF	32	20000-27FFF	32	20000-27FFF
32	50000-57FFF	32	50000-57FFF	32	18000-1FFFF	32	18000-1FFFF
32	48000-4FFFF	32	48000-4FFFF	32	10000-17FFF	32	10000-17FFF
32	40000-47FFF	32	40000-47FFF	32	08000-0FFFF	32	08000-0FFFF
32	38000-3FFFF	32	38000-3FFFF	16	04000-07FFF	4	07000-07FFF
32	30000-37FFF	32	30000-37FFF			4	06000-06FFF
32	28000-2FFFF	32	28000-2FFFF			4	05000-05FFF
32	20000-27FFF	32	20000-27FFF			4	04000-04FFF
32	18000-1FFFF	32	18000-1FFFF	4	03000-03FFF	4	03000-03FFF
32	10000-17FFF	32	10000-17FFF	4	02000-02FFF	4	02000-02FFF
32	08000-0FFFF	32	08000-0FFFF	8	00000-01FFF	4	01000-01FFF
32	00000-07FFF	32	00000-07FFF			4	00000-00FFF

3.4   Command Sets

Command sets are different between the B3 and the LV. The B3 commands are 2-cycle commands whereas LV commands vary between 2 and 6 cycles. Table 7 shows the command sequence differences between the B3 and the LV devices.

To determine which command set to use in an application, the algorithm in Figure 4 may be used to identify which device is in the application through the use of manufacture identifier codes. If the algorithm returns an identification failure, there is another manufacture's device in the socket. Note that this algorithm is dependant on the fact the commands used by the B3 are ignored by the LV and vice versa.

Table 6. Comparison of Intel and AMD Commands

Command	B3 (Addr/Data)	LV (Addr/Data)
Read Mode	XXXXH/FFH	XXXH/F0H
Read ID	XXXXH/90H	5555H/AAH, 2AAAH/55H 5555H/90H
Program	Addr/40H, Addr/Data	5555H/AAH, 2AAAH/55H, 5555H/A0H, Addr/Data
Erase	Blk Addr/20H, Blk Addr/D0H	5555H/AAH, 2AAAH/55H, 5555H/80H, 5555H/AAH 2AAAH/55H, Blk Addr/30H
Erase Suspend	XXXXH/B0H	XXXXH/B0H
Erase Resume	XXXXH/D0H	XXXXH/30H

NOTE:

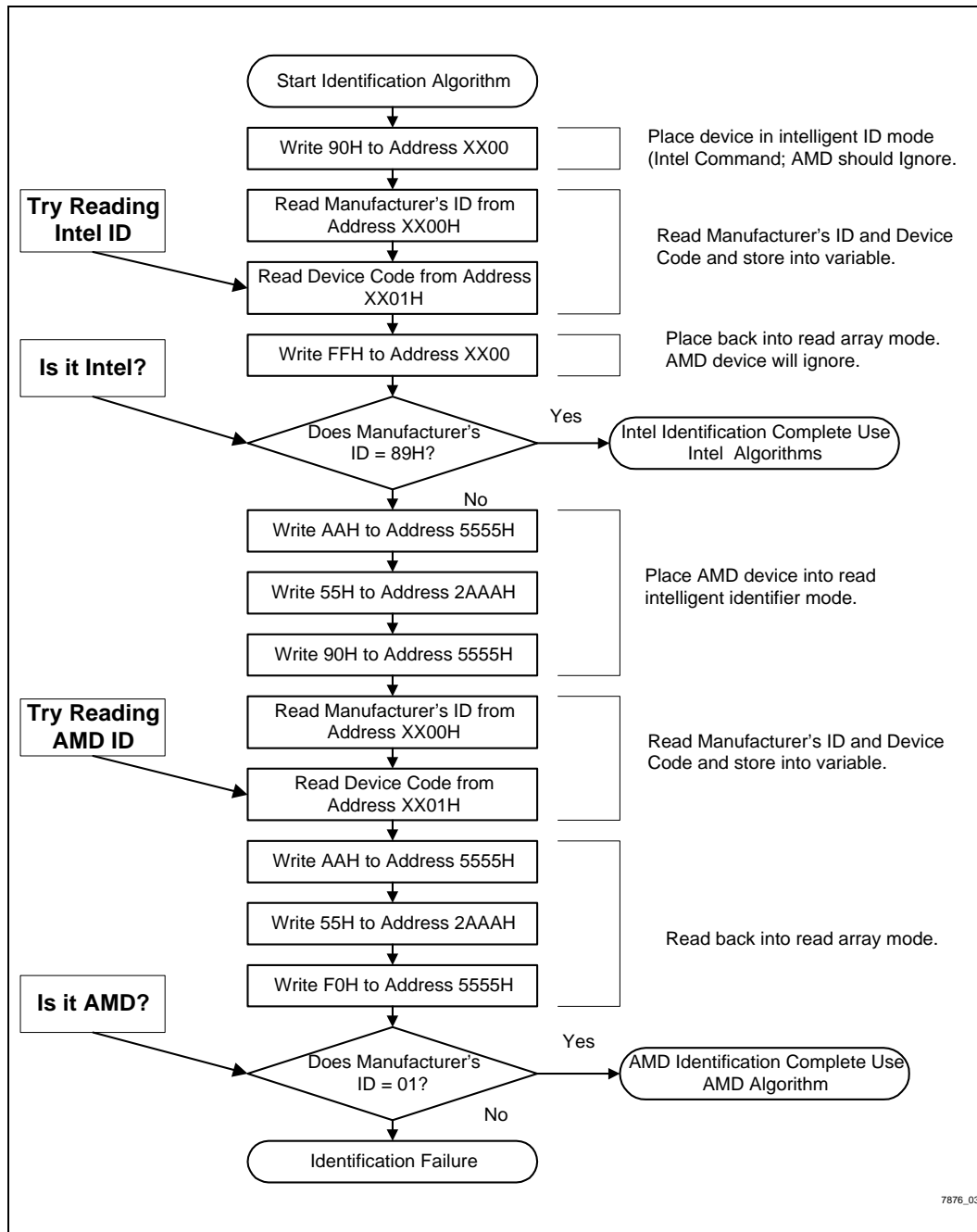Refer to the appropriate datasheet for command definitions.

Figure 4. An Example of Manufacturer Identifier Algorithm

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3.5 Command Completion Changes

B3 devices use a status register for checking operation status while LV devices use the Ready/Busy (RY/BY#) pin to indicate if an operation has be completed. Software should be designed comprehend this difference based on the identification algorithm discussed in Section 3.4.

4.0 SUMMARY

This application note focused on designing a multi-source solution between the B3 and the LV devices. Advantages of designing with the B3 include pinout compatibility for easy upgrade path, 12 Volt production programming for fast programming during manufacturing, program suspend to read functionality for real-time applications, and a vast array of Intel memory managers and design tools to reduce time to market.

To implement a multi-source design, attention is required to AC specifications, pinout differences, blocking differences, command set differences and command completion differences.

APPENDIX A
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290580	*3 Volt Advanced Boot Block Flash Memory; 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3* datasheet
Note 2	*Smart 3 Advanced Boot Block Software Algorithms (Assembly and C Drivers)*
Note 2	Schematic symbols, TimingDesigner* files, VHDL models, Verilog models, and IBIS models

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.

2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.